Objection To The Claims

Claim 12 is objected to by the Examiner for failure to correct the term "reflective index(n)" to read "refractive index (n)". Claim 12 has been amended to alleviate the Examiner's objections. A reconsideration for allowance of claim 12 is respectfully requested of the Examiner.

Claim 9 is objected to for reciting an annealing temperature range between about 400°C and about 1000°C, as conflicting with independent claim 1.

Independent claim 1 has been amended to read "a temperature of at least 400°C". Since claim 1 has been amended to recite dielectric ARC layer of SiO_2 and SiONH only, which are not taught or disclosed by the Plat et al reference. A reconsideration for allowance of claim 9 is respectfully requested of the Examiner.

Claim Rejections Under 35 USC §103

Claims 1-2, 5, 8-11 and 13-16 are rejected under 35 USC §103(a) as being unpatentable over Plat et al '751 in view of Abernathey et al '560. It is contended that while Plat et al teaches all of the limitations of the corresponding claims except

the annealing/heat treating step at a temperature of at least 500°C. It is further contended that Abernathey et al teaches annealing a deposited SiON film in oxygen gas at a temperature between 700°C and 1000°C in order to densify the film.

The rejection of claims 1-2, 5, 8-11 and 13-16 under 35 USC §103(a) based on Plat et al '751 and Abernathey et al is respectfully traversed.

Independent claim 1 has been amended to recite:

"depositing a dielectric ARC layer on said SiN_x or said polysilicon layer **wherein said dielectric ARC layer is deposited of a material selected from the group consisting of SiO_2 and SiONH**".

Independent claim 13 contains similar recitation.

The Applicants respectfully submit that the newly added limitation to independent claims 1 and 13 of either a SiO_2 or a SiONH layer as the dielectric ARC layer is clearly not taught or disclosed by Plat et al nor Abernathey et al, either singularly or

in combination thereof. Plat et al teaches an ARC layer of SiON, while Abernathey et al teaches the use of SiON layer as a storage node dielectric in a capacitor.

The Applicants further submit that Abernathey et al '560 does not teach the present invention method as recited in independent claims 1 and 13 since the process step of depositing SiN_x or polysilicon on a semiconductor substrate is not taught or disclosed. The Abernathey et al's process is limited to the deposition of SiON on a single-crystal silicon substrate as shown at col. 4, lines 38+:

> "The following process was carried out on a clean <100> P-type silicon wafer substrate. The silicon oxynitride is deposited on the substrate by LPCVD techniques to form a thin dielectric layer ..."

In the Abernathey et al's process, there is simply no need for a NT-reflection coating layer since no SiN_x or polysilicon layer is deposited on top of the silicon substrate. The Abernathey et al's process is used for a completely different purpose than the Plat et al's process, and as such, there can be no motivation to combine the two references for a §103 rejection.

The rejection of claims 1-2, 5, 8-11 and 13-16 under 35 USC §103(a) based on Plat et al and Abernathey et al is respectfully traversed. A reconsideration for allowance of claims 1-2, 5, 9-11 and 13-16 is respectfully requested of the Examiner.

Claims 3-4 are rejected under 35 USC §103(a) as being unpatentable over Plat et al in view of Abernathey et al and further in view of Chang et al '146.

Claims 3-4 have been cancelled and withdrawn from further consideration by the Examiner.

Claims 1-2, 6, 8-11 and 13-16 are rejected under 35 USC §103(a) as being unpatentable over Holscher et al '292, in view of Plat et al. It is contended that while Holscher et al does not explicitly teach that an ARC layer is deposited on either a SiN or a polysilicon layer, such is taught by Plat et al in depositing a SiON ARC layer on top of a polysilicon layer.

The rejection of claims 1-2, 6, 9-11 and 13-16 under 35 USC §103(a) based on Holscher et al and Plat et al is respectfully traversed.

The present invention as narrowly recited in independent claims 1 and 13, recites the process step of "depositing a dielectric ARC layer on said SiN_x or said polysilicon layer". The criticality of such process step is only taught by the present invention. As stated in the specification at page 3, line 8 through page 4, line 1:

> "The **surface of a polysilicon layer or a silicon nitride layer is also highly reflective**, almost matching that of an aluminum layer. The high reflectivity of the surface of polysilicon or silicon nitride renders an imaging process for lithography difficult to carry out. The use of an anti-reflective coating layer on top of the polysilicon or the silicon nitride prior to depositing a photoresist layer is therefore necessary. **For compatibility reasons, a dielectric type anti-reflective coating material is more suitable for coating the polysilicon or the silicon nitride surface.**"

The Applicants respectfully submit that neither Holscher nor Plat recognizes such criticality and such use of a dielectric ARC layer, specifically, on a surface of SiNx or polysilicon. Moreover, neither reference teaches the coating of a dielectric ARC layer on SiO_2 or SiONH.

Claims 3-4 are rejected under 35 USC §103(a) as being unpatentable over Holscher et al in view of Plat et al and further in view of Chang et al.

Claims 3-4 have been cancelled and withdrawn from further consideration by the Examiner.

Claims 5, 7 and 17 are rejected under 35 USC §103(a) as being unpatentable over Holscher et al, in view of Plat et al and further in view of Sandhu et al '282. It is contended that while the combination of Holscher and Plat does not teach a method wherein the gas environment used in annealing is O_2, such is taught by Sandhu.

Claims 5 and 7 depend on independent claim 1, while claim 17 depends on independent claim 13. As presented above, the Applicants have clearly shown that independent claims 1 and 13 are not rendered obvious based on Holscher and Plat since neither reference teaches the use of a dielectric ARC layer of SiO_2 or SiONH. The Applicants respectfully submit that the additional reference of Sandhu does not lender any additional weight in a §103 rejection. A reconsideration for allowance of claims 5, 7 and 17 is respectfully requested of the Examiner.

Claim 12 is rejected under 35 USC §103(a) as being unpatentable over Holscher et al, in view of Plat et al and further in view of either Lee '672 or Yao '734.

The rejection of claim 12 under 35 USC §103(a) based on Holscher et al, Plat et al, Lee and Yao is respectfully traversed.

Claim 12 depends on independent claim 1, which the Applicants have clearly shown is not rendered obvious based on the Holscher and Plat references since neither reference teaches the

coating of a dielectric ARC layer of SiO_2 or SiONH. The Applicants therefore respectfully submit that the additional references of Lee and Yao do not lend any additional weight in a §103 rejection based on the Holscher and Plat references. A reconsideration for allowance of claim 12 is respectfully requested of the Examiner.

Based on the foregoing, the Applicants respectfully submit that all of the pending claims, i.e. claims 1-2, 5-7 and 9-17, are now in condition for allowance. Such favorable action by the Examiner at an early date is respectfully solicited.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version With Markings To Show Changes Made".

In the event that the present invention is not in a condition for allowance for any other reasons, the Examiner is respectfully invited to call the Applicants' representative at his

U.S.S.N. 09/761,486

Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for allowance.

Respectfully submitted,

Tung & Associates

Randy W. Tung
Reg. No. 31,311
Telephone: (248) 540-4040

RWT\kd
Attachment: Redline copy of Figs. 4 & 5

U.S.S.N. 09/761,486

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Claims

Please cancel claims 3, 4 and 8.

Claim 1 has been amended as follows:

1. (Twice Amended) A method for adjusting the optical properties of an anti-reflective coating (ARC) layer comprising the steps of:

providing a preprocessed semiconductor substrate having a SiN_x or a polysilicon layer on a top surface;

depositing a dielectric ARC layer on said SiN_x or said polysilicon layer wherein said dielectric ARC layer is deposited of a material selected from the group consisting of SiO_x and SiONH; and

annealing said dielectric ARC layer deposited on said semiconductor substrate at a temperature of at least [500] 400°C [and in a gas comprising at least one element selected from the group consisting of N_2 and O_2].

Claim 2 has been amended as follows:

2. (Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 [further comprising the step of depositing SiON or] wherein said dielectric ARC layer deposited is SiONH [on said SiN_x or said polysilicon layer].

Claim 12 has been amended as follows:

12. (Amended) A method for adjusting the optical properties of an anti-reflective coating layer according to claim 1 further comprising the step of adjusting said optical properties of the dielectric anti-reflective coating layer to a [reflective] refractive index (n) between about 2.0 and about 2.5, and an extinction coefficient (k) between about 0.2 and about 0.8.

Claim 13 has been amended as follows:

13. (Twice Amended) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer by the steps of:

providing a SiN_x or polysilicon layer covered semiconductor substrate;

depositing a dielectric anti-reflective coating layer of a material selected from the group consisting of SiO_2, SiON] and SiONH on top of said SiN_x or said polysilicon layer; and

heating said semiconductor substrate to a temperature between about [500] 400°C and about 1,000°C in an environment that comprises at least one of N_2 or O_2.

Claim 17 has been amended as follows:

17. (Twice Amended) A method for adjusting the extinction coefficient (k) of a dielectric anti-reflective coating layer according to claim 13 further comprising the step of heating said semiconductor substrate to a temperature between [500] 400°C and 700°C in an environment of O_2.